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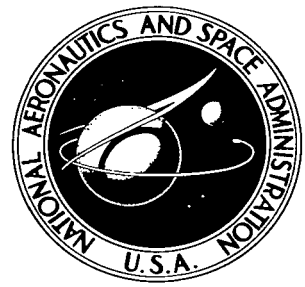

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SOLID-STATE WIDE-RANGE LOW POWER CAMERA TIMER FOR SPACE APPLICATIONS

by Joseph C. Thornwall

Goddard Space Flight Center
Greenbelt, Md.

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ABSTRACT

This paper describes a device for timing sequentially 8 film exposures of a rocket-borne camera with a time interval between each exposure to allow the camera film transport mechanism to step the film from one frame to the next after each exposure. Each exposure time can be independently adjusted from a fraction of a second to several hundred seconds by changing the value of a timing resistor and/or capacitor. All of the rocket interface circuits have been designed to minimize the coupling of spurious noise signals into the timer.

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INTRODUCTION

Rocket-borne camera instruments require a timing control device to open and close the camera shutter several times during a rocket flight. Usually the shutter is opened for a preset period of time for each exposure and is then closed for a sufficient time to advance the film to the next frame before the shutter is reopened. The timer described here was developed to control the shutter of a camera designed to take preset time exposures of the sun during the flight of an Aerobee rocket. The film exposure times varied from a fraction of a second to several hundred seconds with a ±10% tolerance. This tolerance was not more stringent because the actual flight exposure time was telemetered to the ground for use in analyzing the photographs.

The timing devices which are usually employed use either (1) a fixed-frequency-oscillator clock driving a chain of flip-flop scalers, or (2) a variable-frequency-oscillator clock driving a chain of flip-flop scalers with a diode matrix on the scalers to control the frequency of the clock. Each of these systems uses both a relatively high-frequency basic-oscillator clock to determine the minimum timing interval, and a long sequence of flip-flop scalers to obtain a long timing interval. These timing devices have been satisfactory in the past, though they have the disadvantage of relative inflexibility. In the first case, a large number of gates are connected so as to obtain a given timing sequence and timing interval, and it is difficult to change these gates after the timer is fabricated. In the second case, there is a limit to the dynamic range of the single variable-frequency oscillator, and this controls the maximum time obtainable for a given minimum time. The design described in this paper requires fewer gates than does the first method, and provides a greater dynamic range than can be obtained with the second method.

Many of the circuits used in the timer described here were developed at Goddard Space Flight Center for satellite payloads. These circuits require very low average power and have proven quite reliable in satellite instruments.

POWER SUPPLY AND SIGNAL ISOLATION

The camera and low-level electronic circuits for this experiment were mounted in a package at the nose of the rocket, in an attitude controlled ("pointed") section. This experimental pointed

section has a limited space and weight allowance; therefore, the camera shutter timer and experiment battery supply were mounted in a pressurized compartment below the pointed section. This separation introduced an unavoidable ground loop, because the pointed section battery common was connected to the chassis at two points: near the low-level amplifiers in the pointed section, and at the data-handling system's battery supply common in a lower rocket compartment. This ground loop was one source of noise. Other sources were the pulse currents flowing during operation of the shutter and film transport solenoids, the pointed section torque motor, various relays, the rocket timing circuits, and the data handling telemetry transmitter.

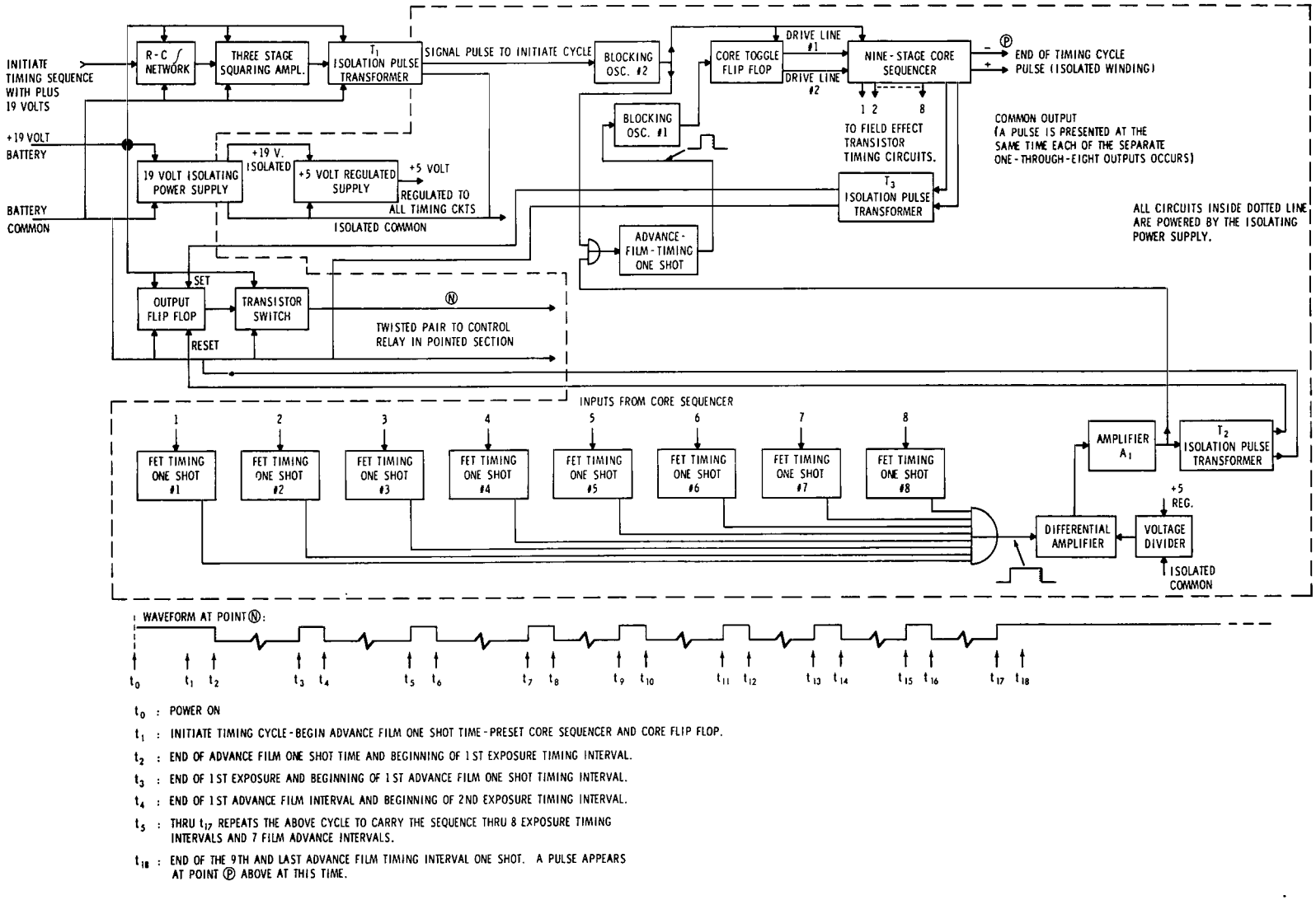
To reduce the coupling of these noise signals into the timer, all of the timing and sequencing circuits were powered from an isolating dc-to-dc converter power supply. In addition, all signal pulses interfacing with the experiment battery and the isolating power supply were coupled through special pulse transformers. These transformers were segment wound to minimize the primary-to-secondary capacitance, thus preventing spurious capacitively-coupled pulses from triggering the timing control circuits.

A complete breadboard circuit was tested to determine the effectiveness of these isolation techniques. A 10-microsecond noise pulse current with a fraction of a microsecond risetime was applied by a pulse generator in series with the battery supply common lead. The peak pulse amplitude available from the signal generator was 5 amperes; and that current, of either polarity, did not spuriously trigger the timer. When the battery and isolation power supply common leads were connected together, the timer did trigger spuriously with the same negative-going pulse at a current of approximately 200 milliamperes. This is a good indication of the effectiveness of the isolation techniques.

BLOCK DIAGRAM OF THE COMPLETE TIMER

Figure 1 is a simplified block diagram of the complete timer, including a waveform diagram showing the voltage signal produced at the output transistor. Electronic circuits in the pointed section were designed both to recognize each positive-going transition in this waveform, i.e. t_3, t_5, etc., and to command the film transport mechanism to step the film one position at each transition. The film advance intervals $t_3 - t_4$, $t_5 - t_6$, etc., were all equal and somewhat longer than the time required to move the film one position. The camera shutter was opened by circuits in the pointed section during the time intervals t_2 to t_3, t_4 to t_5, etc., and the shutter was closed the rest of the time. There are 8 timing intervals in this timer, with the length of each controlled by a separate one-shot timer. These one-shot timers make it possible to control each exposure time interval independently. In the actual unit, timing resistors and capacitors were made accessible so that timing changes could be made up to the time of flight.

The output flip-flop shown in Figure 1 is arranged to have a preferred state when the power is applied to the timer at time t_0. This arrangement assures that the output transistor switch remains off at power turn-on. After a minimum time delay of approximately 6 seconds from power turn-on, the timing cycle is initiated by a voltage applied to the input of the 3-stage squaring



t_0 : POWER ON

t_1 : INITIATE TIMING CYCLE-BEGIN ADVANCE FILM ONE SHOT TIME-PRESET CORE SEQUENCER AND CORE FLIP FLOP.

t_2 : END OF ADVANCE FILM ONE SHOT TIME AND BEGINNING OF 1ST EXPOSURE TIMING INTERVAL.

t_3 : END OF 1ST EXPOSURE AND BEGINNING OF 1ST ADVANCE FILM ONE SHOT TIMING INTERVAL.

t_4 : END OF 1ST ADVANCE FILM INTERVAL AND BEGINNING OF 2ND EXPOSURE TIMING INTERVAL.

t_5 : THRU t_{17} REPEATS THE ABOVE CYCLE TO CARRY THE SEQUENCE THRU 8 EXPOSURE TIMING INTERVALS AND 7 FILM ADVANCE INTERVALS.

t_{18} : END OF THE 9TH AND LAST ADVANCE FILM TIMING INTERVAL ONE SHOT. A PULSE APPEARS AT POINT (P) ABOVE AT THIS TIME.

Figure 1—Rocket experiment timer for camera shutter and film advance control.

amplifier. A minimum time delay is necessary, as will be explained later, because of the behavior of the FET timer one-shots at turn-on. When this voltage is applied, a pulse appears on the secondary of the isolating pulse transformer T1, triggering one-shot blocking oscillator no. 2, which presets the core toggle flip-flop and the core sequencer, and triggers the advance-film timing one-shot. At the end of the advance-film timing one-shot interval, one-shot blocking oscillator no. 1 triggers and drives the core toggle flip-flop, producing a pulse on output drive line no. 1. This output drives a shift line of the core sequencer, and a voltage pulse appearing at core sequencer output no. 1 triggers FET timing one-shot no. 1 and starts the first camera shutter timing interval. A voltage pulse is also generated at this time on the secondary of isolation transformer T_3, triggering the output flip-flop and turning on the output transistor switch (time t_2 in Figure 1).

One side of all of the FET one-shot timing circuits is applied to the input of an "or" gate connected to one input of a differential amplifier (the reason for the differential amplifier will be explained later). At the end of timing interval no. 1, a voltage pulse at the output of amplifier A_1 triggers the advance-film timing one-shot and, through isolating transformer T_2, resets the output flip-flop to turn off the output transistor switch to end the first timing interval (at time t_3). At the end of the advance-film timing one-shot interval, blocking oscillator no. 1 triggers and the cycle continues as a pulse on core sequencer output no. 2 triggers FET timing circuit no. 2. This cycle is repeated with each successive trigger of a FET timing one-shot until the end of the last timing interval (at time t_{17}).

At time t_{17}, the advance-film timing one-shot triggers and the output flip-flop resets for the last time. At the end of the last advance-film timing one-shot interval, a final pulse is applied to the core sequencer and a pulse appears at point P (time t_{18}). However, the output flip-flop is not set at this time since no pulse appears on the secondary of isolating pulse transformer t_3. Furthermore, no core in the core sequencer remains preset (binary "one" state) at the completion of the cycle. Any subsequent triggering of the advance-film timing one-shot will not produce a pulse on any of the core sequencer outputs to start the cycle at the wrong time. More will be said about this in a later section.

FET TIMING ONE-SHOT CIRCUIT

Figure 2 shows a schematic of the FET timing one-shot circuit used in this timer. It is a complimentary-symmetry one-shot with a field effect transistor (FET) in the timing network. The FET has a high input resistance; therefore, a relatively large timing resistance may be used to obtain a much longer delay time

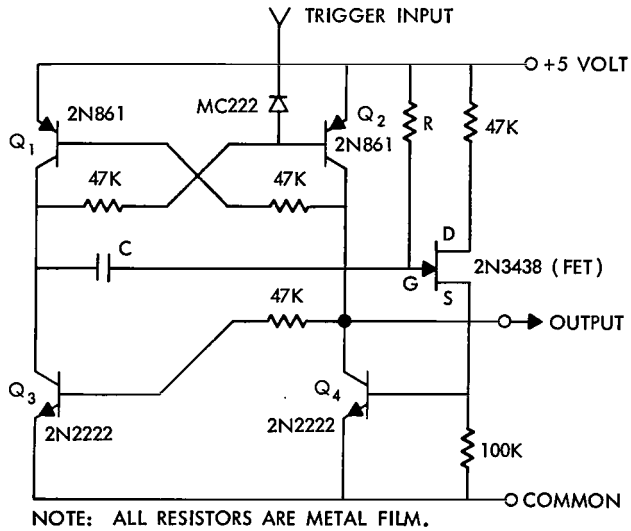


Figure 2—Field effect transistor one-shot circuit.

than is possible for this circuit without the FET. The FET isolates the timing RC elements from transistor Q_4 and provides gain between the junction of R and C and the base of transistor Q_4.

Two undesirable features in the operation of the FET-timing one-shot circuit had to be considered when using it in a practical circuit: (1) the voltage waveform at the trailing edge of the timing interval was not ideal for R-C differentiating, and (2) depending on the length of the timing interval, some time was required for the circuit to become quiescent after the power was applied. The quiescent state is here defined as the state in which transistors Q_4 and Q_1 have turned on, transistors Q_2 and Q_3 have turned off, and capacitor C has charged to its maximum voltage (Figure 2). The voltage waveform at the trailing edge of the timing interval is here defined as the voltage transition (from approximately +5 volts to zero volts) which appears at the output when transistors Q_1 and Q_4 turn on.

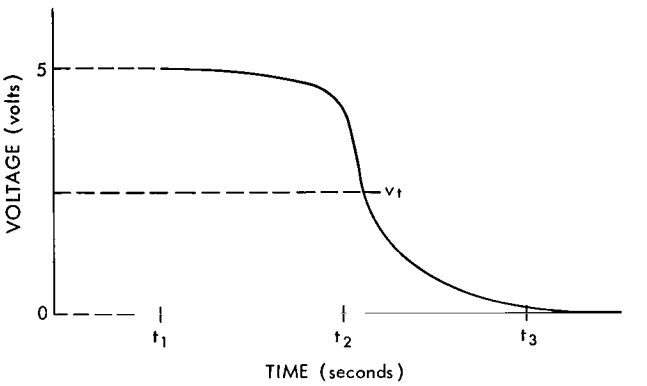


Figure 3—Waveform of the trailing edge of the voltage transient on the output of the field effect transistor one-shot circuit. Time: t_1 to t_2, 6 seconds typical; t_2 to t_3, 150 microseconds typical.

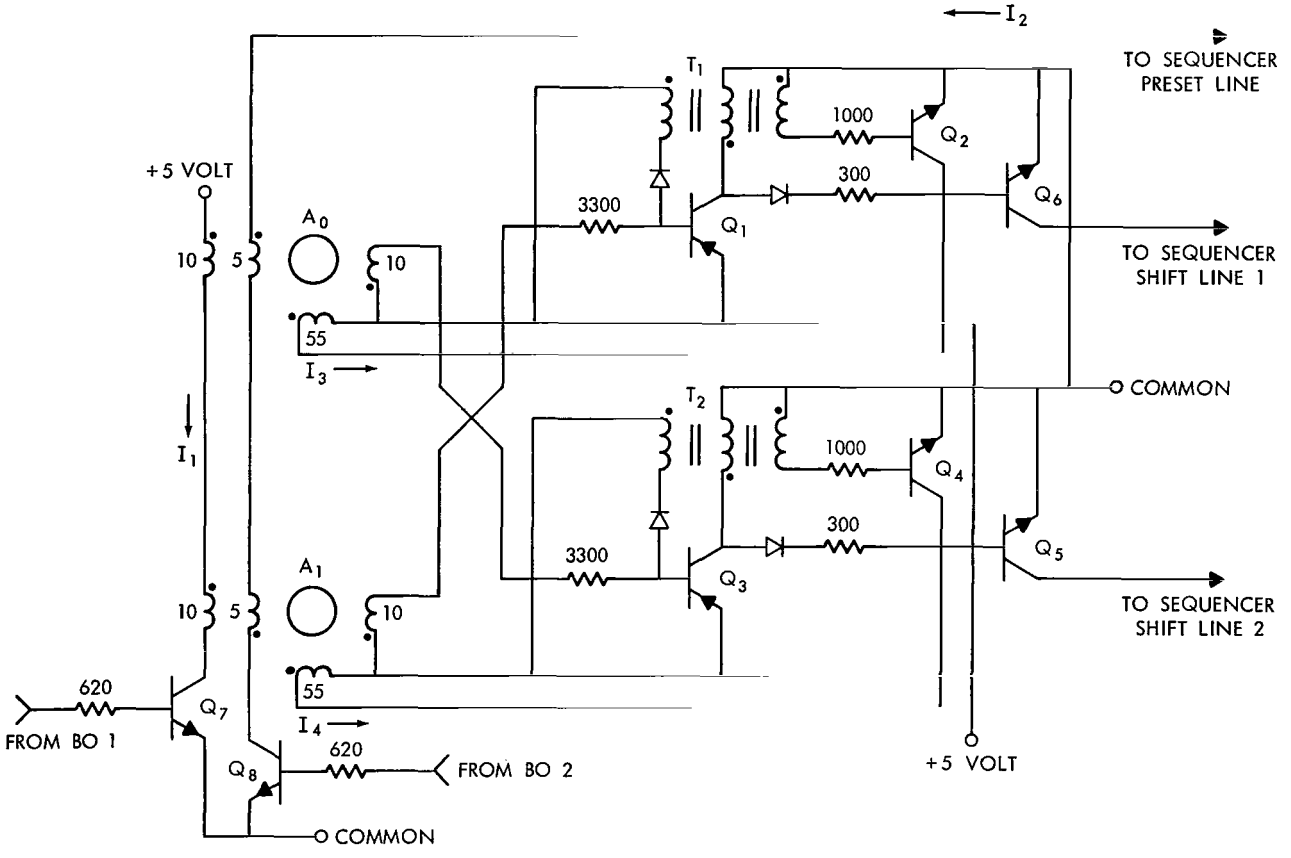
Figure 3 is a drawing of a typical voltage waveform at the trailing edge of a timing interval. A circuit must be made to respond to this waveform in order to define the timing interval, and also to trigger other circuits to continue the timer output voltage waveform. Figure 3 shows that straightforward amplification and squaring of the trailing edge is not a good solution because the interval t_1 to t_2 would require considerable gain to achieve a fast-rising-voltage trigger pulse. Such high gain at this point should be avoided to prevent noise pulse amplification and spurious triggering. A differential amplifier was used to solve this problem: one of its inputs was connected through an "or" gate to the outputs of all 8 FET-timing one-shot circuits, and the other input to a voltage divider. The voltage divider was adjusted so that the differential amplifier changed state at a voltage v_t during the maximum rate-of-change of the voltage transition. Some voltage gain was introduced following the differential amplifier in order to obtain a fast-rising pulse for triggering both the advance-film timing one-shot and the output flip-flop.

If a trigger pulse is derived at the output of the differential amplifier each time a negative-going voltage transition appears on the output of a FET timing one-shot, then some protection must be provided to prevent a spurious timing cycle initiation when the FET timing one-shot becomes quiescent some time after power turn on (approximately 6 seconds in a 100 second timing interval). Since voltage pulses from the core sequencer trigger the FET timing one-shots to continue the timing cycle, the required protection is obtained by an arrangement making it impossible to obtain a pulse from the core sequencer until the timing cycle has been properly initiated by a voltage applied to the "initiate timing cycle" input. This is explained in the description of the core sequencer.

The FET timing one-shot has one additional feature which controls the way in which the timer performs at power turn off and turn on. There is no problem in the timer's normal operation because the power remains turned on until the end of the complete timing cycle. However, when the power is removed, a charge remains on capacitor C which discharges at a rate determined by the RC time constant of the circuit. If the power is reapplied before sufficient time has elapsed to discharge capacitor C completely, the output of the FET timing one-shot will be positive and will remain positive until the charge has been removed and transistor Q_4 turns on. This means that a proper timing cycle cannot be initiated until a minimum time, equal to the longest FET timing one-shot circuit interval, elapses after power turn off. In other words: If the longest timing interval is 100 seconds, then a minimum of 100 seconds must elapse between turn-off and initiation of a new timing cycle, regardless of when the power is reapplied during the intervening interval.

CORE FLIP-FLOP CIRCUIT

Figure 4 is a schematic of the core flip-flop. This circuit requires extremely small average power at the low duty cycle rates of this timer. Its purpose is to provide pulses alternately on



NOTE : ALL NON-LINEAR CORES ARE TAPE WOUND 22 MAXWELL 1/8th MIL MO-PERMALLOY.
ALL LINEAR CORES ARE TAPE WOUND 22 MAXWELL 1 MIL MO-PERMALLOY.
NPN TRANSISTORS ARE 2N2222, PNP TRANSISTORS ARE 2N861, DIODES ARE MC222.
ALL WINDINGS ARE # 40 AWG WIRE.

Figure 4—Core flip-flop circuit.

sequencer shift line nos. 1 and 2, from each pair of pulses applied to the input from blocking oscillator no. 1. The circuit is also arranged so that a pulse occurs on sequencer shift line no. 1 when the first input pulse is applied to the core flip-flop from blocking oscillator no. 1 (BO-1).

The core flip-flop operates in the following way: first a pulse from BO-2 drives transistor switch Q_8 "on", causing a pulse current I_2 to flow from the sequencer through a winding on non-linear core transformers A_0 and A_1. This pulse switches the core of transformer A_0 to the "zero" state and the core of transformer A_1 to the "one" state. Next, a BO-1 pulse drives transistor switch Q_7 "on", causing a pulse current I_1 to flow from +5 volts through a winding on each of the non-linear core transformers A_0 and A_1. This pulse switches the non-linear core of transformer A_1 to the "zero" state, producing a voltage pulse that triggers blocking oscillator transistor Q_1; this in turn drives transistor switch Q_6 "on" and returns sequencer shift line no. 1 to power supply common. The BO-1 pulse that drives transistor switch Q_7 "on" is arranged to be narrower than the pulse obtained from blocking oscillator transformer T_1. After current pulse I_1 has returned to zero, the overshoot voltage from transformer T_1 drives transistor switch Q_2 "on" to produce a pulse current I_3 that switches the non-linear core of transformer A_0 to the "one" state. The next BO-1 pulse drive to transistor switch Q_7 causes the non-linear core of transformer A_0 to switch to the "zero" state, producing a voltage pulse that triggers blocking oscillator transistor Q_3; then Q_3 in turn drives transistor switch Q_5 "on" and returns sequencer shift line 2 to the power supply common. The overshoot voltage from transformer T_2 drives transistor switch Q_4 "on" and switches the non-linear core of transformer A_1 to the "one" state. This cycle is repeated for each pair of BO-1 pulses which alternately switches sequencer shift lines 1 and 2, thus providing the desired two-phase signal to the sequencer.

CORE SEQUENCER

Figure 5 shows a detailed schematic of the core sequencer. The core sequencer provides the following signals: time sequential pulses on 8 separate output lines to trigger the 8 FET one-shots, time sequential pulses on one isolated line pair output to trigger the output flip-flop, and a single pulse that appears only once on another isolated line pair output at the end of the complete timing cycle. This last pulse was not used in the final version of the timer but it was once thought to be necessary. The additional core was thus connected into the core sequencer when it was fabricated. The core sequencer does not allow output pulses to appear before the start of a timing cycle, although spurious input signals may occur at power turn on. The reason for this requirement was discussed previously.

The core sequencer contains 3 series-connected input lines: a preset line connecting all of the cores in series (5 turns per core), one shift line connecting the odd-numbered cores in series (16 turns per core), and another shift line connecting the even-numbered cores in series (16 turns per core). A current pulse on the preset line switches core no. 1 to the "one" state and all of the other cores in this line to the "zero" state. A current pulse on either shift line switches all of the cores on that line to the "zero" state.

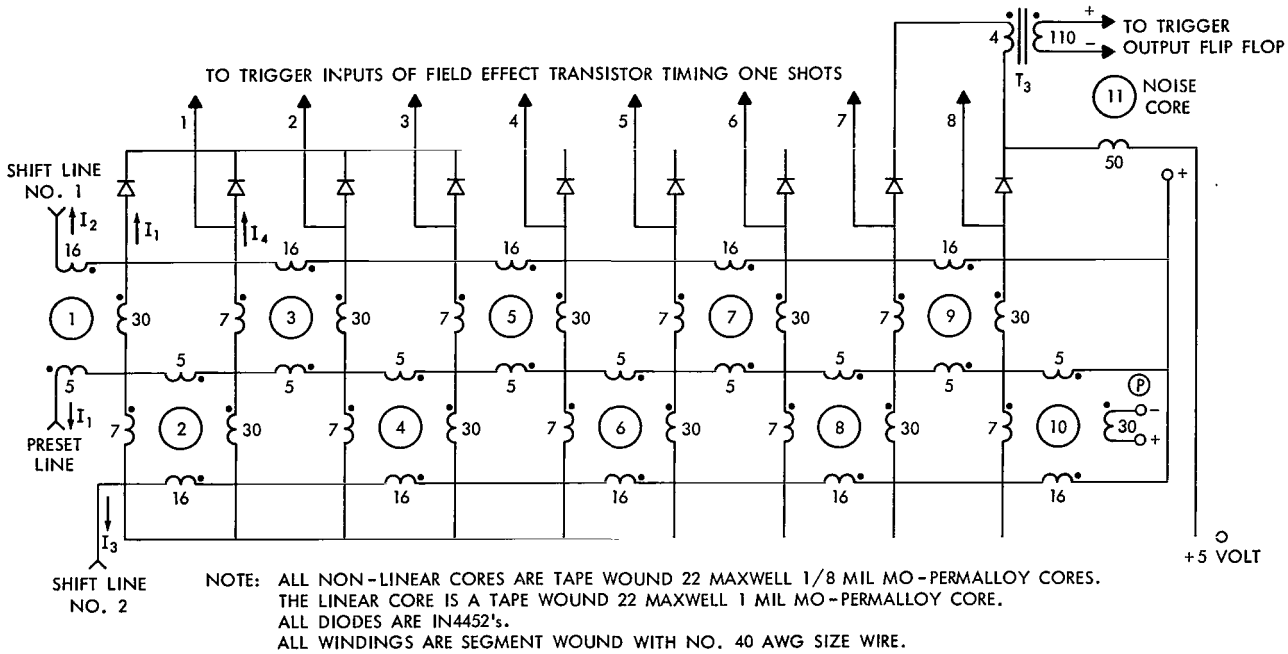


Figure 5—Core sequencer circuit.

The core sequencer will not operate until a pulse is applied to the preset line input. This pulse current (I_1 in Figure 5) switches core no. 1 to the "one" state and switches any other core in the sequencer that may have been in "one" state to the "zero" state, also switching the core of transformer A_1 in the core flip-flop to the "one" state. The current pulse magnitude in this line is adjusted so that any core that switches will require 20 microseconds to do so. As a result, the voltage appearing on the output windings will be very small. This prevents a trigger pulse from appearing at this time on one of the sequencer output lines. Normally, the only cores that will switch at this time are cores no. 1 and 10; the polarity of pulse voltage produced by these cores would cause no harm. However, during the testing of the unit it is sometimes desirable to restart the cycle before it has completed. This will cause the core that was left in the "one" state to return to the "zero" state, and the resulting output voltage could spuriously trigger a one-shot and the output flip-flop. Another reason for this pulse to switch the cores slowly is that this same pulse presets the core flip-flop and, if the core of transformer A_0 switches quickly, transistor Q_3 will trigger, causing shift line no. 2 to be pulsed. This pulse would cause any core sequencer even-numbered core in the "one" state to be switched, thus producing an unwanted trigger pulse. The output pulse voltage produced when these cores switch over a 20 microsecond interval is far below the pulse voltage amplitude required to trigger the one-shot and flip-flop circuit. This assures that no timing circuit will be triggered when the preset pulse is applied.

After the preset line has been pulsed, the next input to the core flip-flop produces a current pulse I_2 in shift line no. 1, switching core no. 1 to the "zero" state and producing a voltage pulse on its 30-turn winding. This voltage pulse produces a current pulse I_1 that flows from the dot side of the 30-turn winding on core no. 1 through a diode, the 4-turn primary winding of transformer

T_3, the 50-turn winding on core 11, the 7-turn winding on core no. 2, and back to the non-dot side of the 30-turn winding. The current pulse I_1 produces (1) a negative-going voltage pulse on the isolated secondary winding of transformer T_3 that triggers the output flip-flop, and (2) a negative-going voltage pulse on the 30-turn winding of core no. 2, as this core switches to the "one" state, that triggers the no. 1 FET one-shot. The voltage pulse from core no. 2 is negative with reference to the +5 volt supply which is the dc voltage applied to the emitter of Q_2 in the FET one shot; thus this point can be direct-coupled through a diode to the base of Q_2. The 50-turn winding on core no. 11 is a convenient way of obtaining an inductance, which is small enough not to affect the current pulse that flows when one of the cores switches from a "one" to a "zero" state, but is large enough to reduce the amplitude of the current pulse generated when the "noise" flux switches in the other cores on the shift line. Core no. 11 eliminates the noise pulse which appears on the outputs of those cores already in the zero state whenever a shift line is pulsed.

The next pulse applied to the input of the core flip-flop causes a current pulse I_3 to appear on shift line no. 2. This pulse switches core no. 2 to the "zero" state, thus producing a current pulse I_4, which causes a voltage to appear both at output no. 2 and the secondary of transformer T_3. This voltage then triggers FET one-shot no. 2 and sets the output flip-flop and continues the cycle, which repeats as each shift line is alternately pulsed, until core no. 10 switches to a "one" state at the end of the last advance-film-timing one-shot interval. The current pulse (produced by core no. 9) that switches core no. 10 does not flow through the primary of transformer T_3, therefore the output flip-flop will not be set by this pulse, and the cycle will end.

An improved FET timing one-shot circuit* has been designed for a later version of this timer. This circuit has an order of magnitude improvement in stability with temperature changes, and in repeatability at a given temperature over the circuit described in this paper.

SPECIFICATIONS

A complete timer schematic, including timing waveforms, is shown in Figure 6. No further comments will be added in the way of explanation of this schematic, because most of the unusual circuits have already been discussed. A paper explaining the 5 volt regulated supply will be published at a later time.

The timer has the following electrical specifications:

1. Input Voltage: +16 to +22 volts. (nominal 19.5 volts).
2. Input current: 5.4 milliamps maximum at nominal voltage.
3. Initiate timing input: 16 volts minimum with a maximum rise time of 10 milliseconds.
4. Maximum load current on output switch: 40 milliamps at nominal power supply voltage.
5. Operating temperature range: -50°C. to +60°C.

*A paper describing the operation of this circuit is being prepared and will appear in a similar publication.

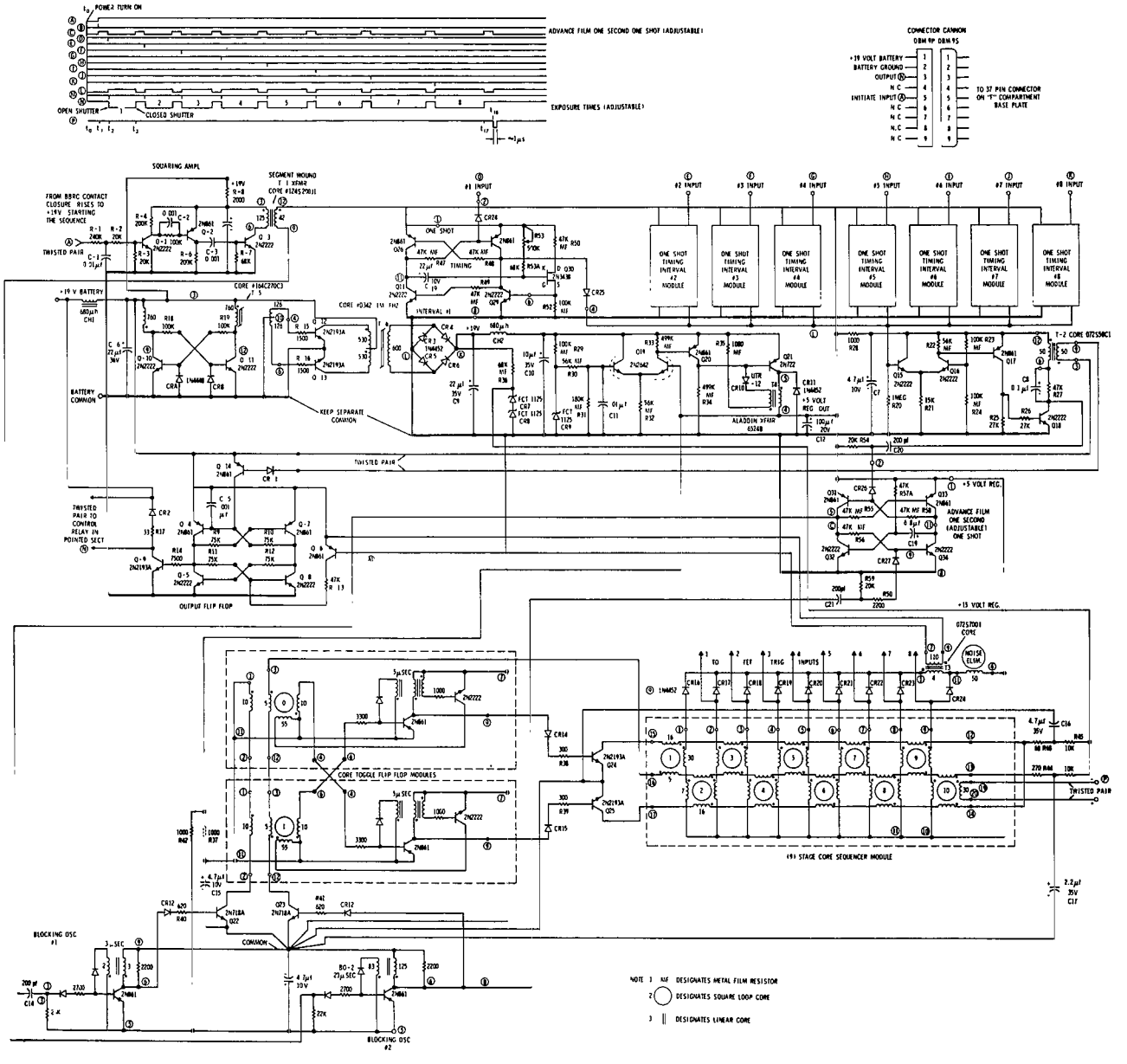


Figure 6—Complete schematic diagram.

6. Timing interval tolerance: ±5% over the operating temperature range.
7. Timing intervals: 8 intervals.
8. Timing period: Each interval independently adjustable from 0.3 seconds to 100 seconds. (This was the range required for this application).
9. Step film period: 1 second ±10%.
10. Pulse at end of timing interval: pulse amplitude 10 volts peak, pulse width 1 microsecond, and output impedance 680 ohms. This pulse appears on an isolated line pair.

The timer has the following mechanical specifications:

1. Height: 2.8"
2. Width: 2.6"
3. Depth: 3.4"
4. Mounting: flange at bottom of unit with 4 mounting screw holes spaced 3-3/4" x 2-1/16." The mounting flange measures 4-1/4" x 2-3/4".
5. Weight: 376 grams.
6. Vibration: 15G, 5 to 2000 cps.

ACKNOWLEDGMENT

The author wishes to acknowledge the assistance of Mr. Gary Harris for his work in the construction and testing of the circuits used in this timer.

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National Aeronautics and Space Administration
Greenbelt, Maryland, July 1, 1966
821-22-03-02-51

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